<u>**REMARKS**</u>

Claims 1, 2, 4-9, 11-15, and 17-20 are presently pending. Claims 3, 10, and 16 are cancelled without prejudice.

Claim 1 was rejected under 35 U.S.C. § 103(a) as being obvious from Wise, Abelard, and Kato. Assignee has amended claim 1 to recite, among other limitations, "logic for determining whether the parameters received by the input are valid, wherein the logic determines whether the parameters received by the input are valid based on the picture type indicator, whether the picture is progressive or interlaced, and the number of motion vectors received by the input".

Assignee respectfully submits that none of Wise, Abelard, or Kato teach "determining whether the parameters received by the input are valid, wherein the logic determines whether the parameters received by the input are valid based on the picture type indicator, *whether the picture is progressive or interlaced*, and the number of motion vectors received by the input".

Claim 5 was rejected under 35 U.S.C. § 103(a) as being obvious from the combination of Wise, Abeland, and Kato in view of Kim. Claim 5 recites, among other limitations, "wherein the control register comprises one or more bits, each of which are associated with a corresponding one or the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector".

Examiner has indicated that Wise, Kato, and Abelard, modified by Kim teaches the foregoing, at [Kim – Abstract; col. 1 lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6, Lines

8-12; col. 5, line 57 - col. 6 line 20]. Kim, Abstract teaches:

> The motion vector decoder includes a parameter delay block which delays transmissions of various input signals necessary for motion vector decoding; a motion vector residual block which extracts a motion residual value and outputs a positive number of the motion residual value; a motion vector code table block which searches for a motion code, a condition of a sign of the motion code, and a zero condition of the motion code using a variable length decoding table and outputting the searched values; a motion vector delta block which calculates a difference of motion vectors from the motion vector residual block and the motion vector code table block; a MV adder which adds the difference value received from the motion vector delta block and a motion vector of a preceding macroblock to output a new motion vector; and a register which updates a flip-flop corresponding to a current (r, s, t) of a new motion vector. The circuit blocks each have at least one flip-flop to allow processing of each block within a single clock.

Although in Kim, Abstract, the "motion vector decoder" includes a number of things, e.g., "a parameter delay block", "a motion vector residual block", "motion vector code table", etc., Kim abstract does not teach anything that "comprises one or more bits, each of which are associated with a corresponding one of the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector".

Moreover, Kim, Col. 6, Lines 8-12 recites that:

> The vlc[10:0], shown in FIG. 2(e), is a MV value variable length coded by the encoder and is received by the MV residual block 11 and the MV code table block. Since maximum of 11 data bits may be produced through the VLC, the vlc[10:0]

> has a length of 11 bits and is the most
> significant bit (msb). The msb value may or may
> not be sent by the encoder and if sent, one or
> all eight values may be sent.

(Emphasis Added). It is noted that Kim does not tech that "vlc[10:0]" "comprises one or more bits, each of which are associated with a corresponding one of the one or more motion vector registers". Moreover, it is noted that "vlc" appears to have 11 bits, "[10:0]", while also indicating that "A maximum of 4 MVs can be obtained per macroblock" at Col. 1, Line 44. Thus vlc[10:0] does not "comprise[s] one or more bits, <u>each of which are associated with a corresponding one of the one or more motion vector registers</u>, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector".

Examiner has also indicated that "Kim discloses 8 bit number in the residual value. [col. 5 line 57 –col. 6 line 20]". Office Action at 2. Assignee has not disputed that Kim discloses "one or more bits", rather, Assignee traverses the finding that Kim discloses one or more bits, <u>each of which are associated with a corresponding one of the one or more motion vector registers</u>, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector". The argument in the above paragraph (it is noted that "vlc" appears to have 11 bits, "[10:0]", while also indicating that "A maximum of 4 MVs can be obtained per macroblock" at Col. 1, Line 44…) would apply the same to 8 bits.

Accordingly, Assignee respectfully traverses the rejection to claim 5 and requests that Examiner withdraw

the rejection to claim 5 and its dependents.

Claim 8 was rejected under 35 U.S.C. § 103(a) as being obvious from Wise, Abelard, and Kato. Claim 8 is amended to recite, among other limitations, "determining the validity of the parameters, wherein determining the validity of the parameters is based on the picture type indicator, whether the picture is interlaced or progressive, whether the picture is frame predicted or field predicted, and the number of motion vectors received".

Assignee respectfully submits that none of Wise, Abelard, and Kato teach the foregoing. Accordingly, Assignee respectfully requests withdrawal of the rejection to claim 8 and its dependents.

Claim 13 was rejected under 35 U.S.C. § 103(a) as being obvious from the combination of Wise, Kato, Abelard, and Kim. Claim 13 is amended to recite, among other limitations "a motion vector address computer for determining the validity of the set of parameters, and calculating addresses associated with motion vectors if the set of parameters are valid, wherein the motion vector address computer determines whether the parameters received by the input are valid based on the picture type indicator, whether the picture is frame predicted, field predicted, dual prime, or 16x8 motion compensation, and the number of motion vectors received by the input".

Assignee respectfully submits that Wise, Kato, Abelard, and Kim does not teach "determines whether the parameters received by the input are valid based on the picture type indicator, whether the picture is frame predicted, field predicted, dual prime, or 16x8 motion compensation, and the number of motion vectors received by the input".

Accordingly, Assignee respectfully requests withdrawal of the rejection to claim 13 and its dependents.

CONCLUSION

For at least the foregoing reasons, Assignee respectfully submits that each of the pending claims are allowable and Examiner is respectfully requested to pass this case to issuance. The Commissioner is hereby authorized to charge additional fees or credit overpayments to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: July 28, 2009   Respectfully submitted,

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